Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A trench field effect transistor (trench-FET) comprising:

a semiconductor body having opposed first and second major surfaces;

a source metallisation at the first major surface; source contact regions of semiconductor doped to have a first conductivity type at the first major surface in contact with the source metallisation;

body contact regions of semiconductor doped to have a second conductivity type opposite to the first conductivity type at the first major surface in contact with the source metallisation;

a drain region of first conductivity type under the first major surface; a drain contact connected to the drain region; and

insulated gates including a conductive gate in an insulated trench for controlling current flow between the source contact region and the drain region through mesa regions between the insulated gates,

wherein the source contact regions and body ~~base~~ contact regions alternate laterally across the first major surface, with the source contact region arranged in the insulated trench above the insulated gate;

wherein the mesa regions comprise doped body regions of semiconductor doped to have the second conductivity type extending under the body contact regions to the drain region, the doped body regions having a lower doping density than the body contact regions.

2. (canceled)

3. (currently amended) A trench-FET according to claim 1 ~~2~~ wherein the source contact

regions extend to a greater depth than the base contact regions so that the source contact regions are in direct contact with the doped body regions under the body contact regions so that current can flow from the source contact regions through the doped body regions past the insulated gate to the drain regions.

4. (currently amended) A trench-FET according claim 1~~2~~, wherein the first conductivity type is n-type and the second conductivity type p-type, the p-type doping of the body contact region being above $5x10^{18}$ cm^{-3}, the p-type doping of the body region being, in the range of $1x10^{17}$ cm^{-3} to $1x10^{18}$ cm^{-3} and the doping of the n-type source contact region being above $1x10^{19}$ cm^{-3}.

5. (previously presented) A trench-FET according to claim 1, wherein the drain regions include a drift region of lower doping above a highly doped drain region of higher doping than the drift region, both drain and drift regions being of the first conductivity type.

6. (previously presented) A trench-FET according to claim 5 wherein the doping in the drift region is below $1x10^{17}$ cm^{-3} and the doping in the highly doped drain region is above $1x10^{18}$ cm^{-3}.

7. (previously presented) A trench-FET according claim 1, wherein the source contact regions extend laterally outside the confines of the trenches as well as above the insulated gate so that the width of the body contact regions between the source contact regions is narrower than the width of the mesa regions between the trenches.

8. (currently amended) A method of manufacturing a trench-FET, including the steps of:

providing a semiconductor body having opposed first and second major surfaces doped to be of first conductivity type to form a drain region;

implanting a body contact region at the first major surface of semiconductor doped to be of a second conductivity type opposite to the first conductivity type;

forming trenches laterally across the first major surface alternating laterally with the body contact regions, the trenches extending below the body contact regions defining mesa regions below the body contact regions between the trenches;

forming insulated gates in the trenches;

depositing source regions of semiconductor doped to be of the first conductivity type in the trenches above the insulated gates; and

depositing a source metallisation at the first major surface contacting the source regions and the body contact regions; and

implanting body regions of second conductivity type to a first depth greater than the depth of the source contact regions wherein the body contact implantation is carried out to a second depth less than the first depth.

9. (canceled)

10. (previously presented) A method according to claim 8 wherein the step of forming insulating gates in the trenches includes the steps of forming insulator on the sidewalls and base of the trenches, forming gate conductor in the trenches to a depth below the top of the trenches and forming gate-source insulator in the trenches above the gate conductor.

11. (new) A trench field effect transistor (trench-FET) comprising:

a semiconductor body having opposed first and second major surfaces;

a source metallisation at the first major surface; source contact regions of semiconductor doped to have a first conductivity type at the first major surface in contact with the source metallisation;

body contact regions of semiconductor doped to have a second conductivity type opposite to the first conductivity type at the first major surface in contact with the source metallisation;

a drain region of first conductivity type under the first major surface; a drain contact connected to the drain region; and

insulated gates including a conductive gate in an insulated trench for controlling current flow between the source contact region and the drain region through mesa regions between the insulated gates,

wherein the source contact regions and body contact regions alternate laterally across the first major surface, with the source contact region arranged in the insulated trench above the insulated gate; and

wherein the source contact regions extend laterally outside the confines of the trenches as well as above the insulated gate so that the width of the body contact regions between the source contact regions is narrower than the width of the mesa regions between the trenches.

12. (new) A trench-FET according to claim 11 wherein the mesa regions comprise doped body regions of semiconductor doped to have the second conductivity type extending under the body contact regions to the drain region, the doped body regions having a lower doping density than the body contact regions.

13. (new) A trench-FET according to claim 12 wherein the source contact regions extend to a greater depth than the base contact regions so that the source contact regions are in direct contact with the doped body regions under the body contact regions so that current can flow from the source contact regions through the doped body regions past the insulated gate to the drain regions.

14. (new) A trench-FET according claim 12, wherein the first conductivity type is n-type and the second conductivity type p-type, the p-type doping of the body contact region being above $5x10^{18}$ cm^{-3}, the p-type doping of the body region being, in the range of $1x10^{17}$ cm^{-3} to $1x10^{18}$ cm^{-3} and the doping of the n-type source contact region being above $1x10^{19}$ cm^{-3}.

15. (new) A trench-FET according to claim 11, wherein the drain regions include a drift region of lower doping above a highly doped drain region of higher doping than the drift region, both drain and drift regions being of the first conductivity type.

16. (new) A trench-FET according to claim 15 wherein the doping in the drift region is below $1x10^{17}$ cm^{-3} and the doping in the highly doped drain region is above $1x10^{18}$ cm^{-3}.